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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,046	08/28/2003	Toru Takayama	0756-7193	7230

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EXAMINER
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NGUYEN, THANH T

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

84

<b>Office Action Summary</b>	<b>Application No.</b> 10/650,046	<b>Applicant(s)</b> TAKAYAMA ET AL.	
	<b>Examiner</b> Thanh T. Nguyen	<b>Art Unit</b> 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on 20 April 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-73 is/are pending in the application.  
     4a) Of the above claim(s) 2,7,12,17,22,27,32 and 58-73 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 36-57 is/are allowed.
- 6) ☒ Claim(s) 1,3-6,8-11,13-16,18-21,23-26,28-31 and 33-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/6/04, 8/28/03</u> | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Election/Restrictions***

Applicant's election of specie I, claims 1, 3-6, 8-11, 13-16, 18-21, 23-26, 28-31, 33-57 in the reply filed on 4/20/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

### ***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119 (a)-(d).

### ***Information Disclosure Statement***

The information disclosure statements filed on 12/6/04, 8/28/03 has been considered.

### ***Oath/Declaration***

Oath/Declaration filed on 12/1/03 has been considered.

*Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-6, 8-10, 21, 23-26, 28-31, 33-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Dairiki (U.S. Patent Publication No. 2002/0061661A1).

Referring to figures 10a-12B, Dairiki teaches a manufacturing method for a semiconductor device, which includes performing heat treatment using a heat source for radiating an incoherent electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band, comprising:

forming a conductive layer (608/609) heated by radiation of the electromagnetic wave (639, see paragraph# 62, 107) over a substrate (see figures: 1, 10, 12);

forming a semiconductor layer (603/604/605) formed inside the conductive layer (608,609) and an insulating layer (607) covering a top surface and a side surface of the semiconductor layer (603/604/605) wherein the semiconductor layer and the insulating layer (607) are interposed between the substrate (601) and the conductive layer ; and

selectively heating a region where the conductive layer is formed, by irradiating the

Art Unit: 2813

electromagnetic wave to thereby conduct the heat treatment on to semiconductor layer and the insulating layer (see figures 1, 10, 12, paragraphs# 62, 107).

Regarding to claim 3, A manufacturing method for a semiconductor device, comprising:  
forming semiconductor layers (603/604/605) that are divided from each other in an island-like shape over a substrate having an insulating surface (see paragraph# 78);  
forming a conductive layer (608/609) covering an entire surface of each of the semiconductor layers and having ends situated outside each of the semiconductor layers, over each of the semiconductor layers through an insulating layer (see figure 10b); and  
selectively heating a region where the conductive layer is formed, by irradiating an incoherent electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band to thereby conduct heat treatment on each of the semiconductor layers and the insulating layer (see figures 1, 10, 12, paragraphs# 62, 107).

Regarding to claim 4, a manufacturing method for a semiconductor device, comprising:  
forming a first insulating layer (602) over a substrate (601) having an insulating surface;  
forming semiconductor layers (603/604/605/606) that are divided from each other in an island-like shape over the first insulating layer (see paragraph# 78);  
forming a second insulating layer (607, see figure 10a) that covers a top surface and a side surface of each of the semiconductor layers;  
forming a conductive layer (608/609, see figure 10b) that covers the top surface and an end surface of each of the semiconductor layers and having ends situated outside each of the semiconductor layers, over the second insulating layer;  
selectively heating a region where the conductive layer is formed, by irradiating an

Art Unit: 2813

incoherent electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band to thereby conduct heat treatment on each of the semiconductor layers and the insulating layer (see figures 1, 10, 12, paragraphs# 62, 107); and

forming a gate electrode (620/621/622/623) overlapping with each of the semiconductor layers by etching the conductive layer (see figure 11a).

regarding to claim 5, a manufacturing method for a semiconductor device, comprising:  
forming semiconductor layers (603/604/605/606) that are divided from each other in an island-like shape over a substrate (see paragraph# 78);

forming a conductive layer (608/609, see figure 10b) covering an entire surface of each of the semiconductor layers and having ends situated outside each of the semiconductor layers, over each of the semiconductor layers through an insulating layer;

irradiating an incoherent electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band for 30 to 300 seconds (see paragraph# 68); and

selectively heating a region where the conductive layer is formed to thereby conduct heat treatment on each of the semiconductor layers and the insulating layer (see figures 1, 10, 12, paragraphs# 62, 68, 107).

Regarding to claims 6, 8, 9, 10, the substrate is glass substrate (see abstract).

Regarding to claims 21, 23, 24, 25, the conductive layer is formed of a metal nitride (tantalum nitride, see paragraph# 82).

Regarding to claims 26, 28, 29, 30, forming a second conductive layer (609) on the conductive layer (608) and forming a part of a gate electrode using the conductive layer (620/621/622/623, see figure 11a-11b).

Regarding to claims 31, 33, 34, 35, the heat treatment is performed at a temperature not less than a distortion point of the substrate (see paragraph# 68, heating at the temperature 1100°C which is greater than 700°C (at the distortion point)).

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims, 11, 13-16, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dairiki (U.S. Patent Publication No. 2002/0061661A1) as applied to claims 1, 3-6, 8-10, 21, 23-26, 28-31, 33-35 above in view of Yamazaki et al. (U.S. Patent Publication No. 2002/0000551).

Dairiki teaches a method of forming a semiconductor device by using a glass substrate. However, Dairiki does not teach the substrate is selected from one of quartz and sapphire, and the substrate has a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band.

Regarding to claims 11, 12, 14, 15, the substrate is selected from one of quartz and sapphire (see paragraph# 237).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form a quartz substrate in process of Dairiki et al. as taught by Yamazaki et al. in order for light transparent or to form an insulating substrate.

Regarding to claims 16, 18, 19, 20, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form the substrate has a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band in process of Dairiki et al. in order to optimize the process.

#### ***Allowable Subject Matter***

Claims 36-57 are allowed. Because none of the prior art alone or in combination teaches a heating the substrate by radiation heating from a first heat source and form the layers on the



Art Unit: 2813

substrate, then heating the layer by using a second heat source for radiating the incoherent electromagnetic wave.

*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).



Thanh Nguyen  
Patent Examiner  
Patent Examining Group 2800

TTN